**In the Claims:**

Please amend claims 1-6 and 9-11 as indicated below. This listing of claims replaces all prior versions.

1. (*Currently Amended*) A method for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit, the method comprising:

providing a constant switch level in a first inverter stage;

providing a variable switch level in ~~the~~ a second inverter stage that depends on a ~~the~~ signal level of the input pad;

comparing the constant switch level of the first inverter stage with the variable switch level of the second stage; and

providing an output signal at an output terminal thereof if the switch level of the second stage is greater than the constant switch level; and

decreasing the switch level of the second inverter stage by an additional circuit element ~~(52)~~ connected in series with the second inverter,

a defined output being produced irrespective of the open circuit condition of ~~an~~ the input pad.

2. (*Currently Amended*) A fail-safe circuit for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit, the fail-safe circuit comprising:

a first inverter stage providing a constant switch level;

a second inverter stage providing a variable switch level that depends ~~of the~~ on a signal level of the input pad and comparing the constant switch level of the first inverter stage with the variable switch level of the second stage and providing an output signal at an output terminal thereof if the variable switch level of the second stage is greater than the constant switch level; and

an additional circuit element connected in series with the second inverter for decreasing the switch level of the second inverter stage;

wherein the fail-safe circuit produces a defined output irrespective of the open circuit condition of the input pad.

3. (*Currently Amended*) The circuit of claim 2, wherein the first inverter stage ~~is a~~ includes at least two transistors each having a gate electrode and a drain electrode ~~stage~~, and wherein the gate electrodes and the drain electrodes of the at least two transistors ~~of the first inverter stage~~ are connected to each other.

4. (*Currently Amended*) The circuit of claim 2, wherein the second inverter stage ~~is a~~ includes at least two transistors each having a gate electrode and a drain electrode ~~stage~~, and wherein the gate electrodes of the at least two transistors ~~of the second inverter stage~~ are connected to each other and wherein the drain electrodes of the at least two transistors are connected to each other.

5. (*Currently Amended*) The circuit of claim 2, wherein ~~the~~ gate electrodes of the second inverter stage are connected to ~~the~~ gate electrodes of the first inverter stage.

6. (*Currently Amended*) The circuit of claim 2, wherein the input ~~terminal~~ pad is connected to a source electrode of the second inverter stage.

7. (*Previously Presented*) The circuit of claim 2, wherein the output terminal is connected to a drain electrode of the second inverter stage.

8. (*Previously Presented*) The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode.

9. (*Currently Amended*) The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode, ~~where the gate of~~ the transistor having a gate that is connected to ~~the~~ VCC and ~~the~~ a source that is connected to ground, the ~~defined~~ output signal being a high level signal.

10. (*Currently Amended*) The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode, ~~where the gate of~~ the transistor having a gate that is connected to ground and ~~the~~ a source that is connected to VCC, the ~~defined~~ output signal being a low level signal.

11. (*Currently Amended*) A digital circuit unit comprising an input terminal, a pull-up stage, a fail-safe stage for producing a fail-safe output signal in case of an open circuit condition of the input terminal, a signal processing stage and an output terminal, wherein the fail-safe stage comprises: ~~the features of claim 2~~

a first inverter stage providing a constant switch level,

a second inverter stage providing a variable switch level that depends on a signal level of the input terminal and comparing the constant switch level of the first inverter stage with the variable switch level of the second stage and providing an output signal at the output terminal if the variable switch level of the second stage is greater than the constant switch level, and

an additional circuit element connected in series with the second inverter for decreasing the switch level of the second inverter stage;

wherein the fail-safe circuit produces a defined output irrespective of the open circuit condition of the input terminal.